



**UNITED STATES DEPARTMENT OF COMMERCE  
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/435,766 11/08/99 KUSHIDA T 104361

MMC1/0808

OLIFF & BERRIDGE PLC  
PO BOX 19928  
ALEXANDRIA VA 22320

EXAMINER

LOKE, S

ART UNIT

PAPER NUMBER

2811

DATE MAILED:

08/08/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

# Office Action Summary

Application No.  
09/435,766

Applicant(s)  
Kushida

Examiner  
Loke

Art Unit  
2811



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Jun 4, 2001
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-4 and 12 is/are pending in the application.
- 4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12 is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some\* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

- 15) ☐ Notice of References Cited (PTO-892) 18) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 19) ☐ Notice of Informal Patent Application (PTO-152)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_ 20) ☐ Other: \_\_\_\_\_

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1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Terashima.

In regards to claim 1, Terashima shows all the elements of the claimed invention in figs. 1 and 14. It is a semiconductor device, comprises: an electrode [10]; a region [2] having a first conductive type (p-type) and disposed on the electrode [10]; a region [1] having a second conductive type (n-type) and disposed on the p-type region [2]; a channel region [1] (protruding portion [3]) having the second conductive type (n-type) and disposed on the region [1]; a gate region [6] provided so as to surround at least a part of the channel region [1] via an insulation film [5]; a region [4] having the second conductive type (n-type) provided on the channel region [1], the region [4] is located substantially at a center of the channel region [1], and the region [4] is isolated from the insulation film [5]; and an electrode [9] connected to the region [4].

In regards to claim 3, Terashima shows a semiconductor region [13] having the first conductive type (p-type) provided between the channel region [1] and the electrode [9].

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

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such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terashima.

In regards to claim 2, it would have been obvious for the gate region has the first conductive type (p-type) because it is a conventional gate electrode material.

In regards to claim 2, Terashima shows a depletion layer is formed over most of the entire channel region when a predetermined voltage is applied to the gate region (col. 8, lines 5-16).

In regards to claim 4, Terashima shows a semiconductor region [13] having the first conductive type (p-type) provided between the channel region [1] and the electrode [9].

5. Claim 12 is allowed.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920.

sl

August 7, 2001

Steven Loke  
Primary Examiner

